

# 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash

## SST25WF512 / SST25WF010 / SST25WF020



Advance Information

### FEATURES:

- **Single Voltage Read and Write Operations**
  - 1.65-1.95V
- **Serial Interface Architecture**
  - SPI Compatible: Mode 0 and Mode 3
- **High Speed Clock Frequency**
  - 40MHz
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Ultra-Low Power Consumption:**
  - Active Read Current: 9 mA (typical @ 20MHz)
  - Standby Current: 2  $\mu$ A (typical)
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 32 KByte overlay blocks
  - Uniform 64 KByte overlay blocks (2 Mbit only)
- **Fast Erase and Byte-Program:**
  - Chip-Erase Time: 125 ms (typical)
  - Sector-/Block-Erase Time: 62ms (typical)
  - Byte-Program Time: 50  $\mu$ S (typical)
- **Auto Address Increment (AAI) Programming**
  - Decrease total chip programming time over Byte\_Program operations
- **End-of-Write Detection**
  - Software polling the BUSY bit in Status Register
  - Busy Status readout on SO pin
- **Reset Pin (RST#) or Programmable Hold Pin (HOLD#) option**
  - Hardware Reset pin as default
  - Hold pin option to suspend a serial sequence without deselecting the device
- **Write Protection (WP#)**
  - Enables/Disables the Lock-Down function of the status register
- **Software Write Protection**
  - Write protection through Block-Protection bits in status register
- **Temperature Range**
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
- **Packages Available**
  - 8-lead SOIC (150 mils)
- **All non-Pb (lead-free) devices are RoHS compliant**

### PRODUCT DESCRIPTION

The SST25WF512/010/020 are members of the Serial Flash 25 Series family and features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. SST25WF512/010/020 SPI serial flash memories are manufactured with SST proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST25WF512/010/020 devices significantly improve performance and reliability, while lowering power consumption. The devices write (Program or Erase) with a single

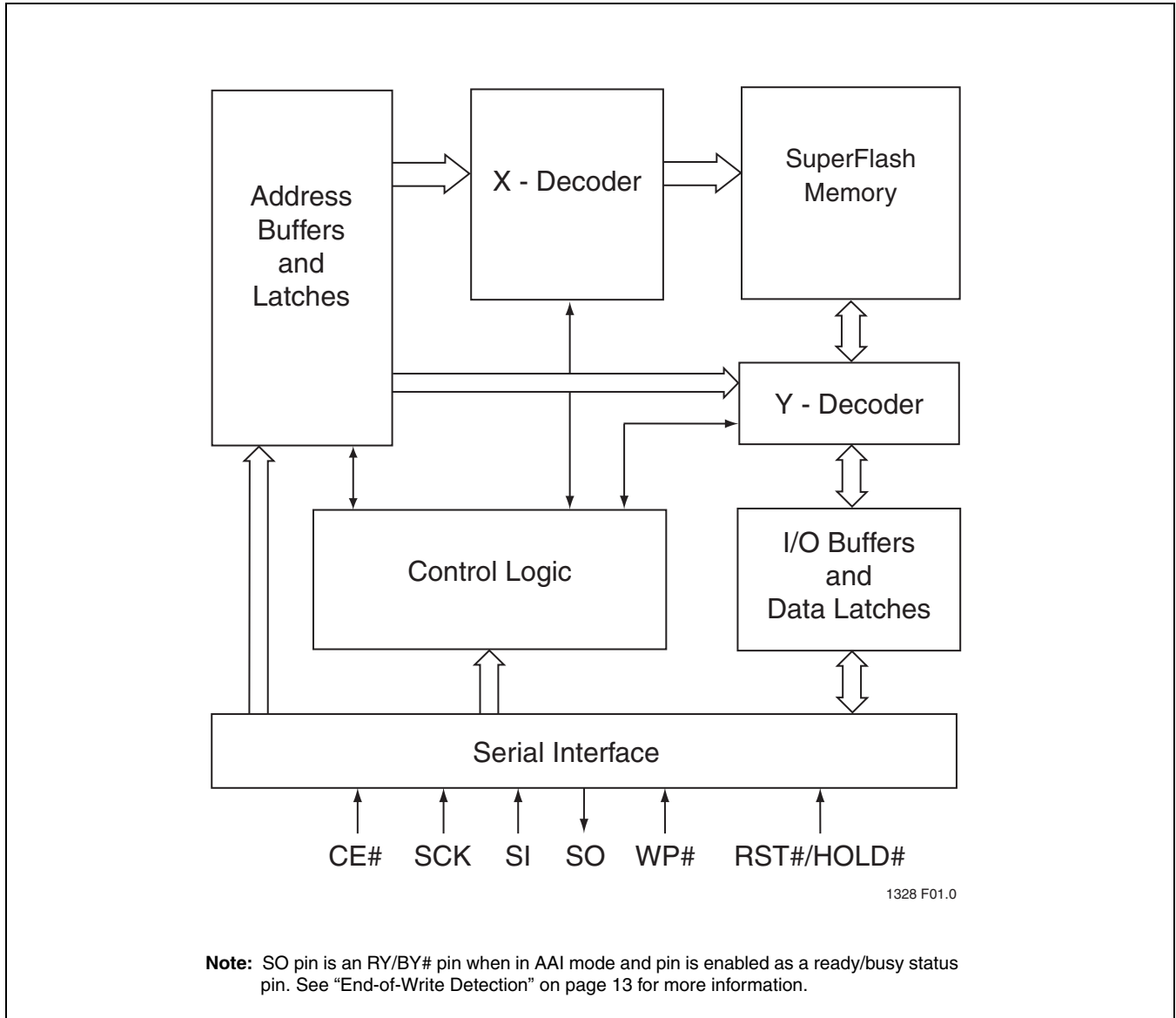
power supply of 1.65-1.95V for SST25WF512/010/020. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SST25WF512/010/020 devices are offered in an 8-lead, 150 mils SOIC package. See Figure 2 for the pin assignment.



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**FIGURE 1: Functional Block Diagram**

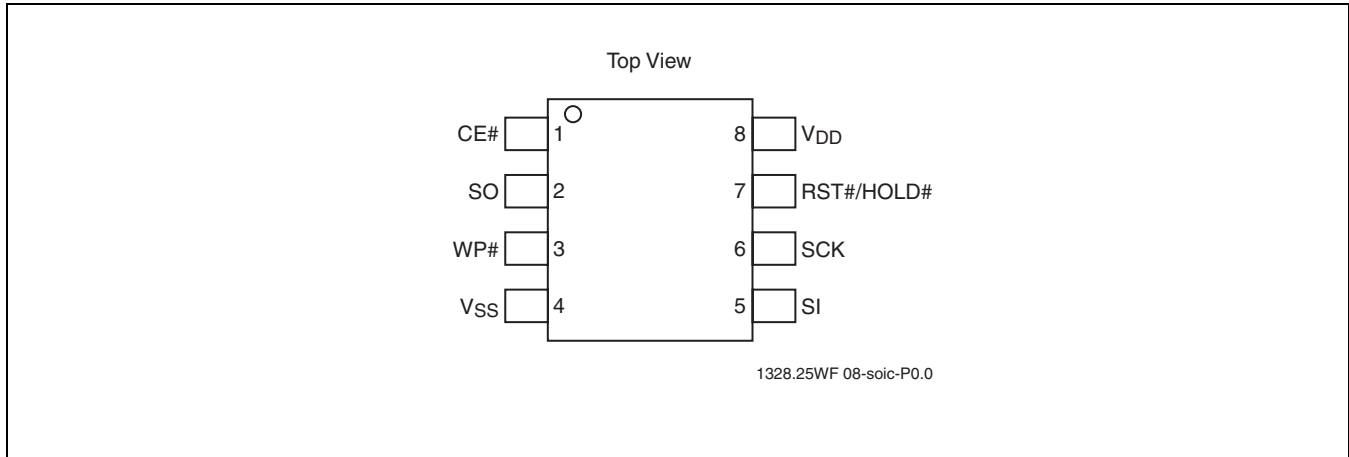


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## SST25WF512 / SST25WF010 / SST25WF020

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### PIN DESCRIPTION



**FIGURE 2: Pin Assignment for 8-Lead SOIC**

**TABLE 1: Pin Description**

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. The SO pin is an RY/BY# pin when in AAI mode and the pin is enabled as a ready/busy status pin. See "End-of-Write Detection" on page 13 for more information.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
RST#/HOLD#	Reset	To reset the operation of the device and the internal logic. The device powers on with RST# pin functionality as default.
	Hold	To temporarily stop serial communication with SPI Flash memory while device is selected. This is selected by an instruction sequence which is detailed in Reset/Hold Mode section on page 10.
V <sub>DD</sub>	Power Supply	To provide power supply voltage: 1.65-1.95V for SST25WF512/010/020
V <sub>SS</sub>	Ground	

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## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

### Advance Information

### MEMORY ORGANIZATION

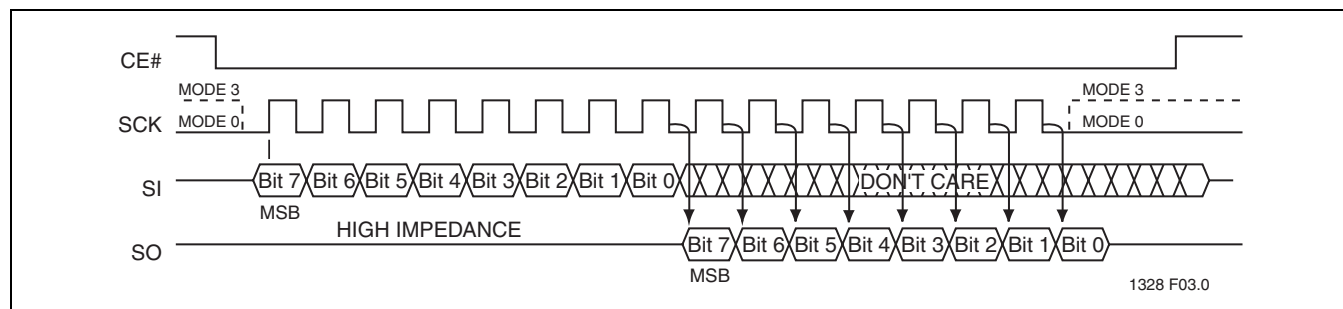
The SST25WF512/010/020 SuperFlash memory arrays are organized in uniform 4 KByte with 16 KByte, 32 KByte, and 64 KByte (2Mbit Only) overlay erasable blocks.

### DEVICE OPERATION

The SST25WF512/010/020 are accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines; Chip Enable (CE#) is

used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The SST25WF512/010/020 support both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 3, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.



**FIGURE 3: SPI Protocol**



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### Reset/Hold Mode

The RST#/HOLD# pin provides either a hardware reset or a hold pin. From power-on, the RST#/HOLD# pin defaults as a hardware reset pin (RST#). The Hold mode for this pin is a user selected option where an Enable-Hold instruction is initiated to enter the Hold mode. Once selected as a hold pin (HOLD#), the RST#/HOLD# pin will be configured as a HOLD# pin, and goes back to RST# pin only after a power-off and power-on sequence.

### Reset

If the RST#/HOLD# pin is used as a reset pin, RST# pin provides a hardware method for resetting the device. Driving the RST# pin high puts the device in normal operating

mode. The RST# pin must be driven low for a minimum of  $T_{RST}$  time to reset the device. The SO pin is in high impedance state while the device is in reset. A successful reset will reset the status register to its power-up state. See Figure 4 for default power-up modes. A device reset during an active Program or Erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation. The device exits AAI Programming Mode in progress and places the SO pin in high impedance state.

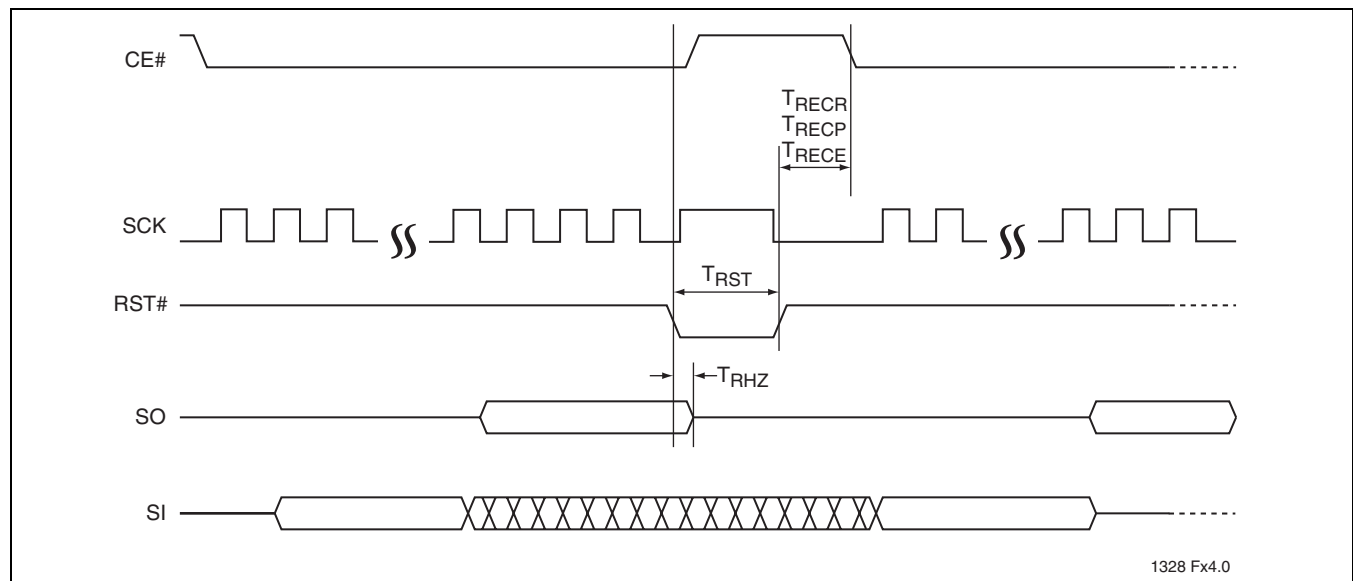


FIGURE 4: Reset Timing Diagram

TABLE 2: Reset Timing Parameters

Symbol	Parameter	Min	Max	Units
$T_{RST}$	Reset Pulse Width	100		ns
$T_{RHZ}$	Reset to High-Z Output		107	ns
$T_{RECR}$	Reset Recovery from Read		100	ns
$T_{RECP}$	Reset Recovery from Program		10	$\mu$ s
$T_{RECE}$	Reset Recovery from Erase		1	ms

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## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

### Advance Information

#### Hold

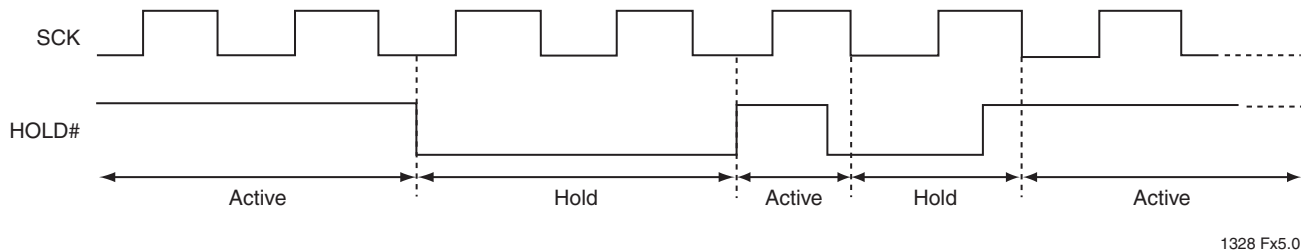
The Hold operation enables the hold pin functionality of the RST#/HOLD# pin. Once set to hold pin mode, the RST#/HOLD# pin continues functioning as a hold pin until the device is powered off and then powered on. After a power-off and power-on, the pin functionality returns to a reset pin (RST#) mode. See “Enable-Hold (EHL D)” on page 19 for detailed timing of the Hold instruction.

In the hold mode, serial sequences underway with the SPI Flash memory are paused without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the rising edge of the HOLD# signal coincides with the SCK active low state. If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters

Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 5 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be  $V_{IL}$  or  $V_{IH}$ .

If CE# is driven active high during a Hold condition, the device returns to standby mode. The device can then be re-initiated with the command sequences listed in Tables 8 and 9. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 5 for Hold timing.



**FIGURE 5: Hold Condition Waveform**

#### Write Protection

SST25WF512/010/020 provide software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the status register. The Block-Protection bits (BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 5 for the Block-Protection description.

#### Write Protect Pin (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP# is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 3). When WP# is high, the lock-down function of the BPL bit is disabled.

**TABLE 3: Conditions to execute Write-Status-Register (WRSR) Instruction**

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

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## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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### Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the Memory Write protection. During an internal Erase or

Program operation, the status register may be read only to determine the completion of an operation in progress. Table 4 describes the function of each bit in the software status register.

**TABLE 4: Software Status Register**

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 5)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 5)	1	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP1 and BP0 are read-only bits 0 = BP1 and BP0 are read/writable	0	R/W

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#### Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. A '1' for the Busy bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

#### Auto Address Increment (AAI)

The Auto Address Increment Programming-Status bit provides status on whether the device is in AAI programming mode or Byte-Program mode. The default at power up is Byte-Program mode.

#### Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal Write-Enable-Latch memory. If the WEL bit is set to '1', it indicates the device is Write enabled. If the bit is set to '0' (reset), it indicates the device is not Write enabled and does not accept any Write (Program/Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Reset instruction completion
- Power-up
- Write-Disable (WRDI) instruction completion
- Byte-Program instruction completion
- Auto Address Increment (AAI) programming is completed or reached its highest unprotected memory address
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Status-Register instructions



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#### Block Protection (BP1, BP0)

The Block-Protection (BP1, BP0) bits define the size of the memory area to be software protected against any memory Write (Program or Erase) operation, see Table 5. The Write-Status-Register (WRSR) instruction is used to program the BP1 and BP0 bits as long as WP# is high or the Block-Protect-Lock (BPL) bit is '0'. Chip-Erase can only be executed if Block-Protection bits are all '0'. After power-up, BP1 and BP0 are set to defaults. See Table 4 for defaults at power-up.

#### Block Protection Lock-Down (BPL)

When the WP# pin is driven low ( $V_{IL}$ ), it enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP1, and BP0 bits. When the WP# pin is driven high ( $V_{IH}$ ), the BPL bit has no effect and its value is 'Don't Care'. After power-up, the BPL bit is reset to '0'.

**TABLE 5: Software Status Register Block Protection for SST25WF512**

Protection Level	Status Register Bit		Protected Memory Address
	BP1 <sup>1</sup>	BP0	512 Mbit
None	0	0	None
1 (Upper Quarter Memory)	0	1	0C000H-0FFFFH
2 (Upper Half Memory)	1	0	08000H-0FFFFH
3 (Full Memory)	1	1	00000H-0FFFFH

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1. Default at power-up for BP1 and BP0 is '11'.

**TABLE 6: Software Status Register Block Protection for SST25WF010**

Protection Level	Status Register Bit		Protected Memory Address
	BP1 <sup>1</sup>	BP0	1 Mbit
None	0	0	None
1 (Upper Quarter Memory)	0	1	018000H-01FFFFH
2 (Upper Half Memory)	1	0	010000H-01FFFFH
3 (Full Memory)	1	1	000000H-01FFFFH

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1. Default at power-up for BP1 and BP0 is '11'.

**TABLE 7: Software Status Register Block Protection for SST25WF020**

Protection Level	Status Register Bit		Protected Memory Address
	BP1 <sup>1</sup>	BP0	2 Mbit
None	0	0	None
1 (Upper Quarter Memory)	0	1	030000H-03FFFFH
2 (Upper Half Memory)	1	0	020000H-03FFFFH
3 (Full Memory)	1	1	000000H-03FFFFH

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1. Default at power-up for BP1 and BP0 is '11'.





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### INSTRUCTIONS

Instructions are used to read, write (Erase and Program), and configure the SST25WF512/010/020. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Page-Program, Auto Address Increment (AAI) programming, Sector-Erase, Block-Erase, Write-Status-Register, or Chip-Erase instructions, the Write-Enable (WREN) instruction must be executed first. The complete list of instructions is provided in Table 8. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge

of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

**TABLE 8: Device Operation Instructions for SST25WF512 and SST25WF010**

Instruction	Description	Op Code Cycle <sup>1</sup>	Address Cycle(s) <sup>2</sup>	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	20 MHz
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	40 MHz
4 KByte Sector-Erase <sup>3</sup>	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0	
32 KByte Block-Erase <sup>4</sup>	Erase 32 KByte block of memory array	0101 0010b (52H)	3	0	0	
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Byte-Program	To Program One Data Byte	0000 0010b (02H)	3	0	1	
AAI-Word-Program <sup>5</sup>	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞	
RDSR <sup>6</sup>	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	
EWSR	Enable-Write-Status-Register	0110 0000b (50H)	0	0	0	
WRSR <sup>7</sup>	Write-Status-Register	0000 0001b (01H)	0	0	1	
WREN	Write-Enable	0000 0110b (06H)	0	0	0	
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	
RDID <sup>8</sup>	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞	
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 000b (70H)	0	0	0	
DBSY	Disable SO to output RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0	
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞	
EHLD	Enable HOLD# pin functionality of the RST#/HOLD# pin	1010 1010b (AAH)	0	0	0	

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- One bus cycle is eight clock periods.
- Address bits above the most significant bit of each density can be  $V_{IL}$  or  $V_{IH}$ .
- 4 KByte Sector-Erase addresses: use  $A_{MS}-A_{12}$ , remaining addresses are don't care but must be set either at  $V_{IL}$  or  $V_{IH}$ .
- 32 KByte Block-Erase addresses: use  $A_{MS}-A_{15}$ , remaining addresses are don't care but must be set either at  $V_{IL}$  or  $V_{IH}$ .
- To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0=0$ , Data Byte 1 will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0 = 1$ .
- The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
- This command is for backward compatibility to SST 25VF/LF series, user should use WRSR for new designs
- Manufacturer's ID is read with  $A_0=0$ , and Device ID is read with  $A_0=1$ . All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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**TABLE 9: Device Operation Instructions for SST25WF020**

Instruction	Description	Op Code Cycle <sup>1</sup>	Address Cycle(s) <sup>2</sup>	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	20 MHz
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	40 MHz
4 KByte Sector-Erase <sup>3</sup>	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0	
32 KByte Block-Erase <sup>4</sup>	Erase 32 KByte block of memory array	0101 0010b (52H)	3	0	0	
64 KByte Block-Erase <sup>5</sup>	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0	
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Byte-Program	To Program One Data Byte	0000 0010b (02H)	3	0	1	
AAI-Word-Program <sup>6</sup>	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞	
RDSR <sup>7</sup>	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	
EWSR	Enable-Write-Status-Register	0110 0000b (50H)	0	0	0	
WRSR <sup>8</sup>	Write-Status-Register	0000 0001b (01H)	0	0	1	
WREN	Write-Enable	0000 0110b (06H)	0	0	0	
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	
RDID <sup>9</sup>	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞	
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 000b (70H)	0	0	0	
DBSY	Disable SO to output RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0	
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞	
EHLD	Enable HOLD# pin functionality of the RST#/HOLD# pin	1010 1010b (AAH)	0	0	0	

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- One bus cycle is eight clock periods.
- Address bits above the most significant bit of each density can be  $V_{IL}$  or  $V_{IH}$ .
- 4 KByte Sector-Erase addresses: use  $A_{MS}-A_{12}$ , remaining addresses are don't care but must be set either at  $V_{IL}$  or  $V_{IH}$ .
- 32 KByte Block-Erase addresses: use  $A_{MS}-A_{15}$ , remaining addresses are don't care but must be set either at  $V_{IL}$  or  $V_{IH}$ .
- 64 KByte Block-Erase addresses: use  $A_{MS}-A_{16}$ , remaining addresses are don't care but must be set either at  $V_{IL}$  or  $V_{IH}$ .
- To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0=0$ , Data Byte 1 will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0 = 1$ .
- The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
- This command is for Backward compatibility to SST 25VF/LF series, user should use WRSR for new designs.
- Manufacturer's ID is read with  $A_0=0$ , and Device ID is read with  $A_0=1$ . All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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### Read (20 MHz)

The Read instruction, 03H, supports up to 20 MHz Read. The device outputs a data stream starting from the specified address location. The data stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wrap-

around) of the address space. For example, for 2 Mbit density, once the data from the address location 3FFFFH is read, the next output is from address location 000000H. The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits  $A_{23}-A_0$ . CE# must remain active low for the duration of the Read cycle. See Figure 6 for the Read sequence.

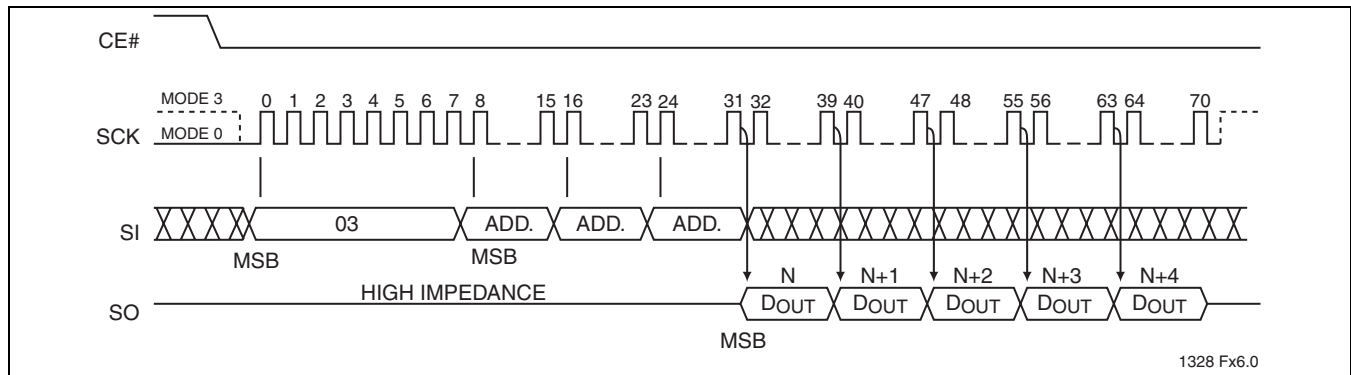


FIGURE 6: Read Sequence

### High-Speed-Read (40 MHz)

The High-Speed-Read instruction supporting up to 40 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits  $[A_{23}-A_0]$  and a dummy byte. CE# must remain active low for the duration of the High-Speed-Read cycle. See Figure 7 for the High-Speed-Read sequence.

Following a dummy cycle, the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all

addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, for 2 Mbit density, once the data from address location 3FFFFH is read, the next output will be from address location 000000H.

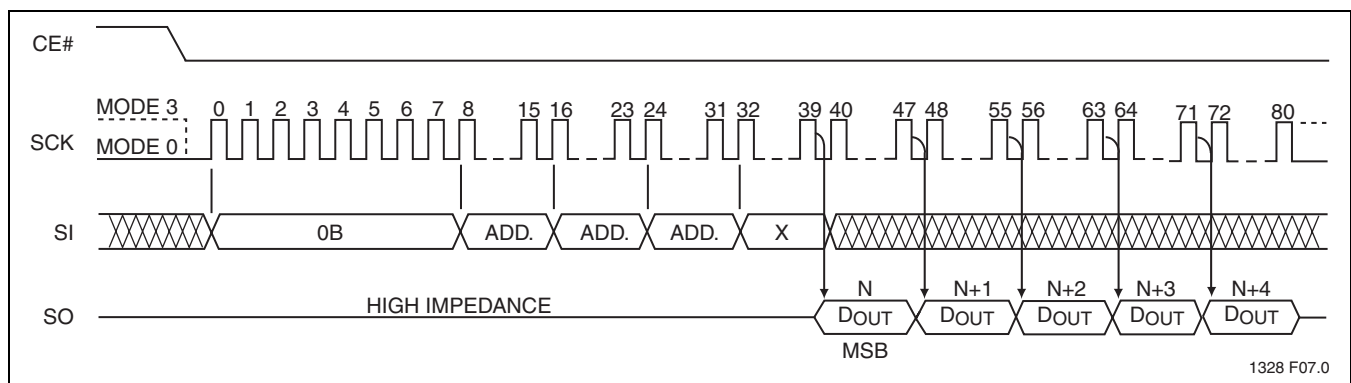


FIGURE 7: High-Speed-Read Sequence



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

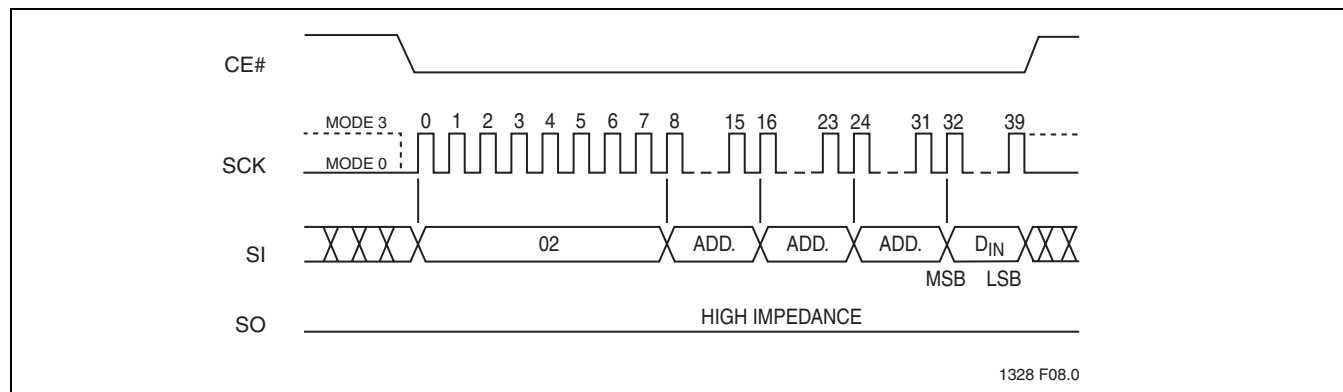
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### Byte-Program

The Page-Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte-Program instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Page-Program instruction. The Byte-

Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the address, the data is input in order from MSB (bit 7) to LSB (bit 0). CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T<sub>BP</sub> for the completion of the internal self-timed Byte-Program operation. See Figure 8 for the Page-Program sequence.



**FIGURE 8: Byte-Program Sequence**



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### Auto Address Increment (AAI) Word-Program

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when multiple bytes or entire memory array is to be programmed. An AAI Word program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI Word Program operation. While within AAI Word Programming sequence, the only valid instructions are AAI Word (ADH), RDSR (05H), or WRDI (04H). Users have three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software status register or wait  $T_{BP}$ . Refer to End-Of-Write Detection section for details.

Prior to any write operation, the Write-Enable (WREN) instruction must be executed. The AAI Word Program instruction is initiated by executing an 8-bit command, ADH, followed by address bits  $[A_{23}-A_0]$ . Following the addresses, two bytes of data is input sequentially, each one from MSB (Bit 7) to LSB (Bit 0). The first byte of data (D0) will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0 = 0$ , the second byte of Data (D1) will be programmed into the initial address  $[A_{23}-A_1]$  with  $A_0 = 1$ . CE# must be driven high before the AAI Word Program instruction is executed. The user must check the BUSY status before entering the next valid command. Once the device indicates it is no longer busy, data for the next two sequential addresses may be programmed and so on. When the last desired byte had been entered, check the busy status using the hardware method or the RDSR instruction and execute the Write-Disable (WRDI) instruction, 04H, to terminate AAI. Check the busy status after WRDI to determine if the device is ready for any command. See Figures 11 and 12 for AAI Word programming sequence.

There is no wrap mode during AAI programming; once the highest unprotected memory address is reached, the device will exit AAI operation and reset the Write-Enable-Latch bit ( $WEL = 0$ ) and the AAI bit ( $AAI = 0$ ).

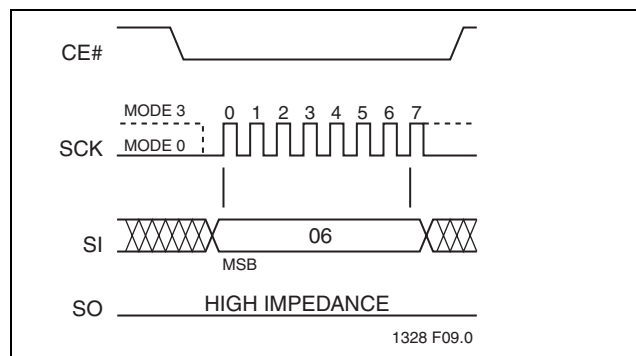
### End-of-Write Detection

There are three methods to determine completion of a program cycle during AAI Word programming: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the Software Status Register or wait  $T_{BP}$ .

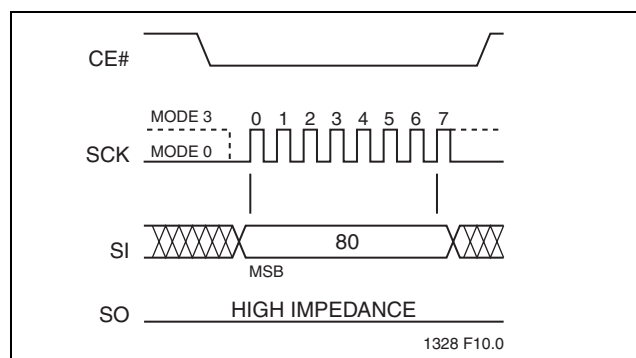
### Hardware End-of-Write Detection

The Hardware End-of-Write detection method eliminates the overhead of polling the Busy bit in the Software Status Register during an AAI Word program operation. The 8-bit command, 70H, configures the Serial Output (SO) pin to indicate Flash Busy status during AAI Word programming, as shown in Figure 9. The 8-bit command, 70H, must be executed prior to executing an AAI Word-Program instruction. Once an internal programming operation begins, asserting CE# will immediately drive the status of the internal flash status on the SO pin. A '0' indicates the device is busy and a '1' indicates the device is ready for the next instruction. De-asserting CE# will return the SO pin to tri-state.

The 8-bit command, 80H, disables the Serial Output (SO) pin to output busy status during AAI-Word-program operation and re-configures SO as an output pin. Once SO is an output pin, allows the use of RDSR instruction for polling during AAI Word Programming; and Software Status Register data outputs through the SO pin. This is shown in Figure 10.



**FIGURE 9: Enable SO as Hardware RY/BY# during AAI Programming**

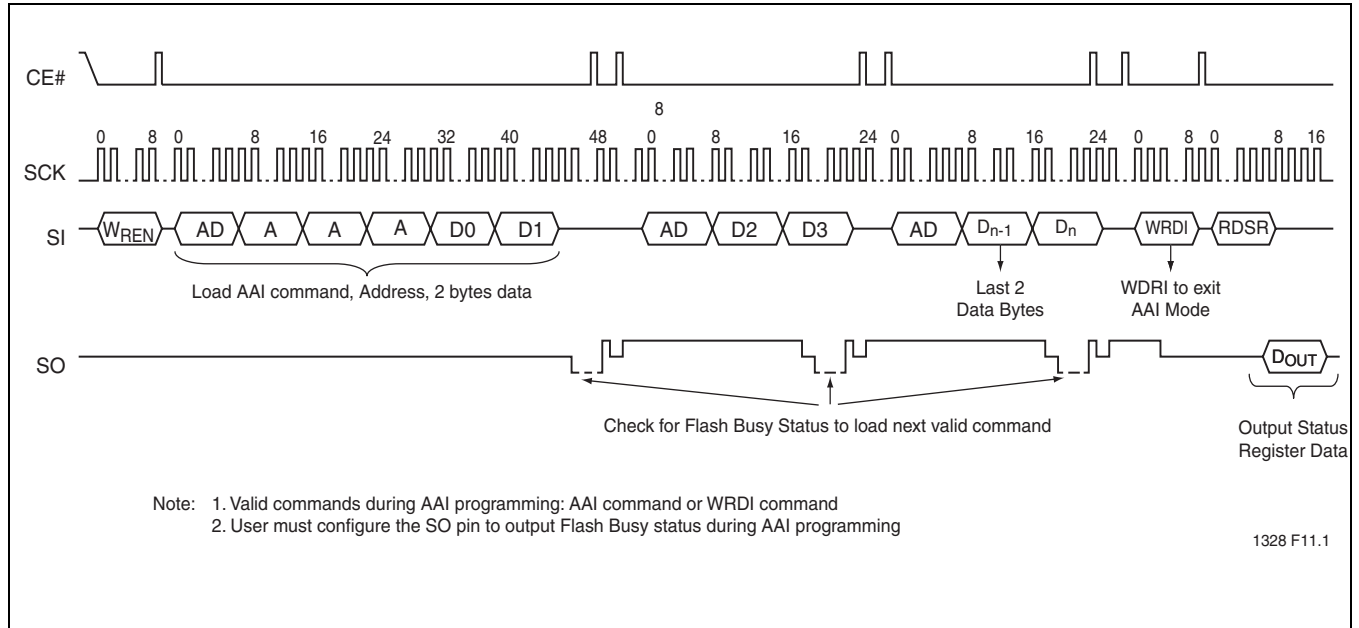


**FIGURE 10: Disable SO as Hardware RY/BY# during AAI Programming**

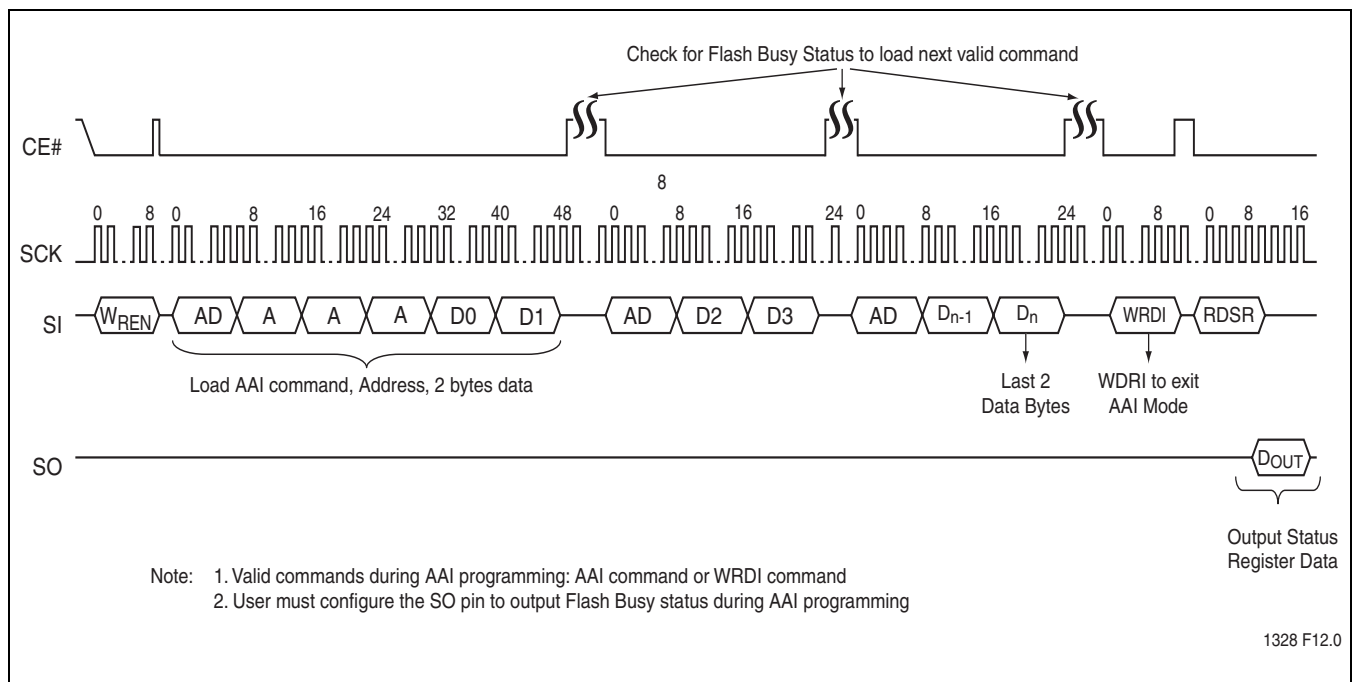


# 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

## Advance Information



**FIGURE 11: Auto Address Increment (AAI) Word Program Sequence with Hardware End-of-Write Detection**



**FIGURE 12: Auto Address Increment (AAI) Word Program Sequence with Software End-of-Write Detection**



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

Advance Information

### Sector-Erase

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>12</sub>] (A<sub>MS</sub> = Most

Significant address) are used to determine the sector address (SA<sub>X</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T<sub>SE</sub> for the completion of the internal self-timed Sector-Erase cycle. See Figure 13 for the Sector-Erase sequence.

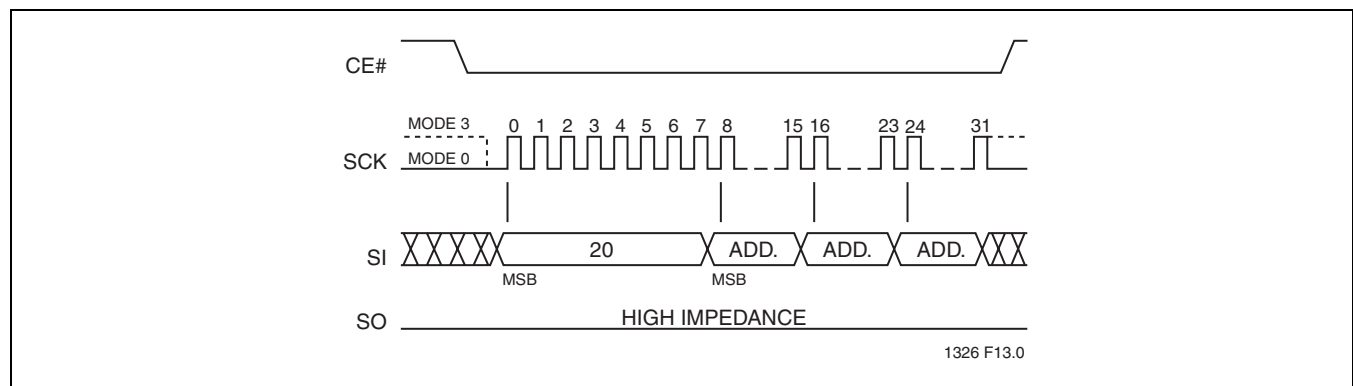


FIGURE 13: Sector-Erase Sequence

### 32-KByte Block-Erase

The Block-Erase instruction clears all bits in the selected 32 KByte block to FFH. A Block-Erase instruction applied to a protected memory area is ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Block-Erase instruction is initiated by executing an 8-bit command, 52H, followed by

address bits [A<sub>23</sub>-A<sub>0</sub>]. Address bits [A<sub>MS</sub>-A<sub>15</sub>] (A<sub>MS</sub> = Most Significant Address) are used to determine block address (BA<sub>X</sub>), remaining address bits can be V<sub>IL</sub> or V<sub>IH</sub>. CE# must be driven high before the instruction is executed. Poll the Busy bit in the software status register or wait T<sub>BE</sub> for the completion of the internal self-timed Block-Erase. See Figures 14 and 15 for the Block-Erase sequences.

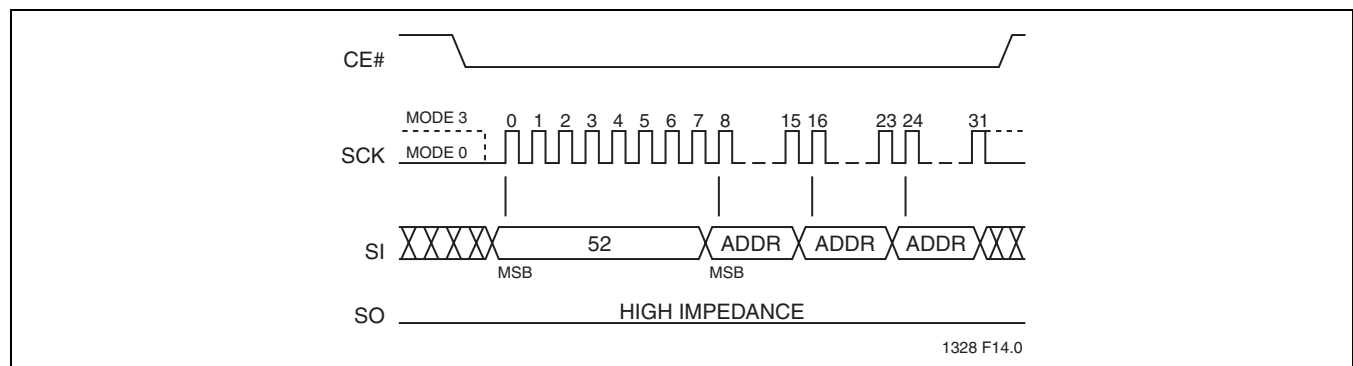


FIGURE 14: 32-KByte Block-Erase Sequence



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

### Advance Information

#### 64-KByte Block-Erase for SST25WF020

The Block-Erase instruction clears all bits in the selected 64 KByte block to FFH. A Block-Erase instruction applied to a protected memory area is ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Block-Erase instruction is initiated by executing an 8-bit command, 52H, followed by

address bits  $[A_{23}-A_0]$ . Address bits  $[A_{MS}-A_{16}]$  ( $A_{MS}$  = Most Significant Address) are used to determine block address ( $BA_x$ ), remaining address bits can be  $V_{IL}$  or  $V_{IH}$ . CE# must be driven high before the instruction is executed. Poll the Busy bit in the software status register or wait  $T_{BE}$  for the completion of the internal self-timed Block-Erase. See Figures 14 and 15 for the Block-Erase sequences.

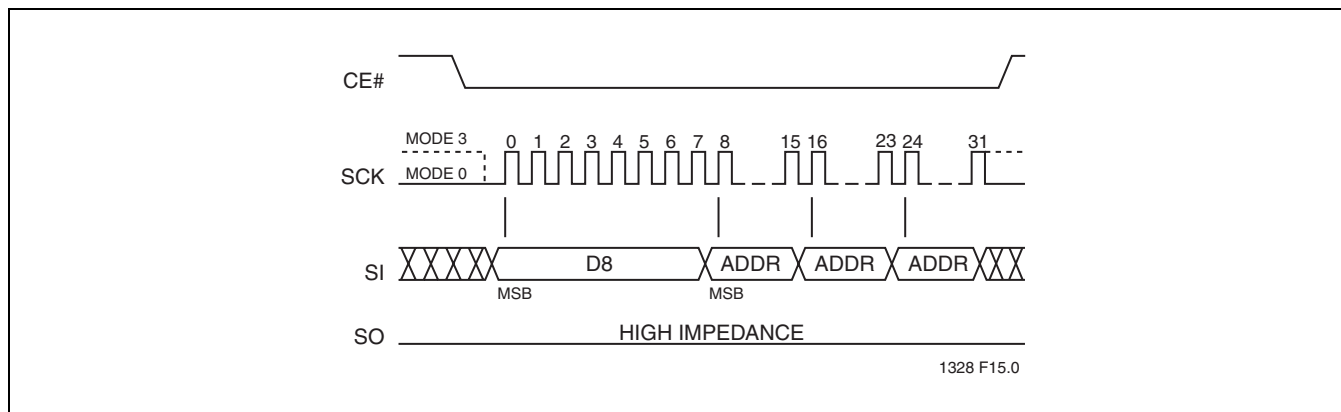


FIGURE 15: 64-KByte Dual-Block-Erase Sequence

#### Chip-Erase

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction is ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Chip-Erase instruction sequence. The Chip-Erase instruction is initiated

by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait  $T_{CE}$  for the completion of the internal self-timed Chip-Erase cycle. See Figure 16 for the Chip-Erase sequence.

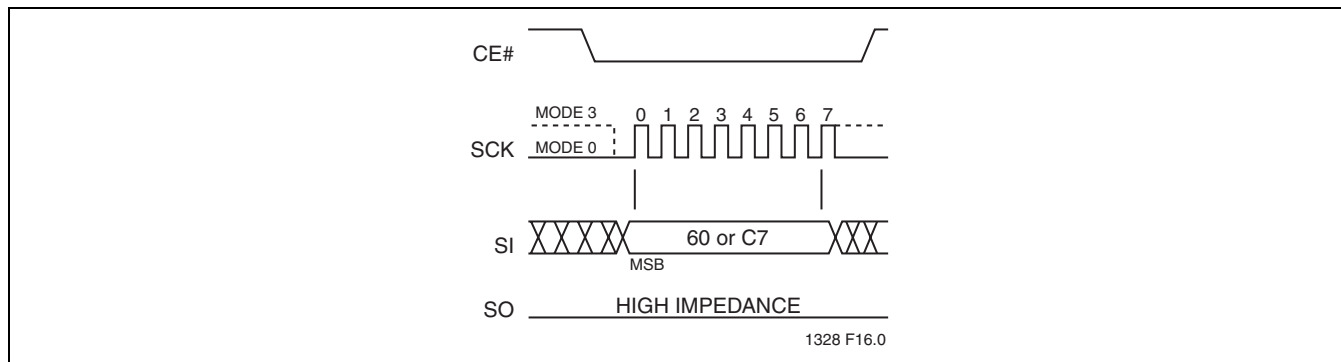


FIGURE 16: Chip-Erase Sequence





## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

Advance Information

### Read-Status-Register (RDSR)

The Read-Status-Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation. When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the CE#. See Figure 17 for the RDSR instruction sequence.

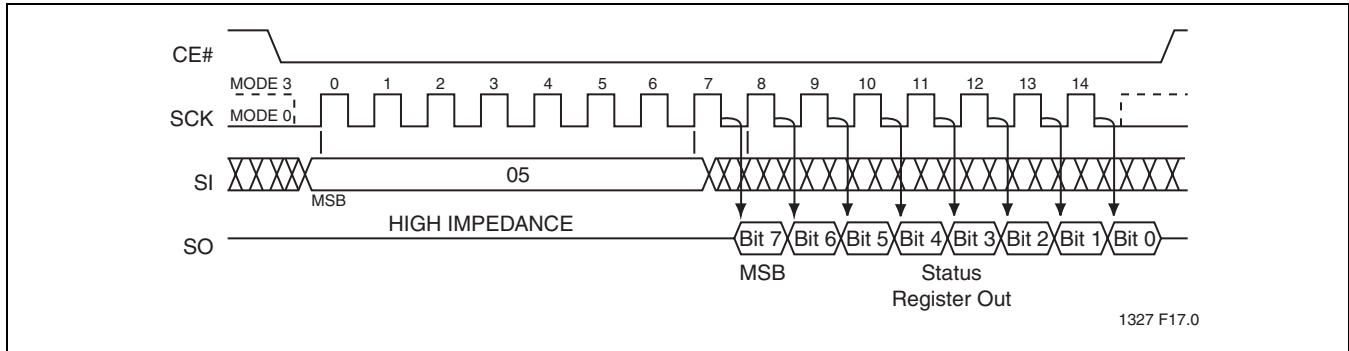


FIGURE 17: Read-Status-Register (RDSR) Sequence

### Write-Enable (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit in the Status Register to 1 allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow execution of

the Write-Status-Register (WRSR) instruction; however, the Write-Enable-Latch bit in the Status Register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

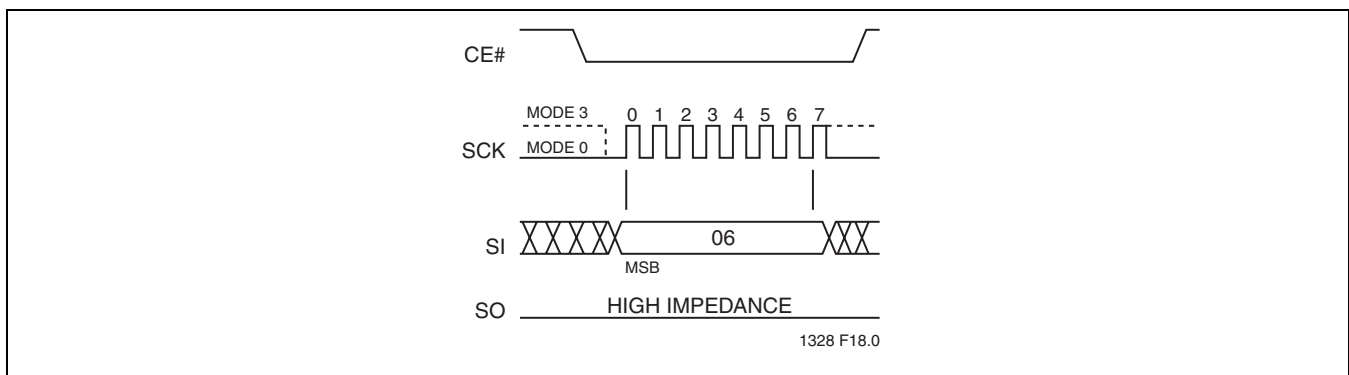


FIGURE 18: Write Enable (WREN) Sequence



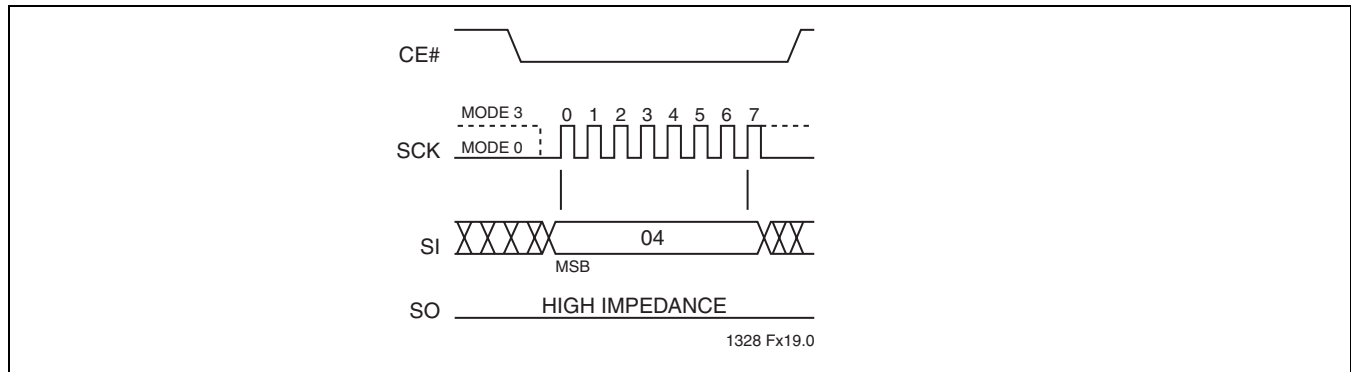
## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

### Advance Information

#### Write-Disable (WRDI)

The Write-Disable (WRDI) instruction resets the Write-Enable-Latch bit and AAI to 0 disabling any new Write operations from occurring. The WRDI instruction will not terminate any programming operation in progress. Any pro-

gram operation in progress may continue up to  $T_{BP}$  after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.



**FIGURE 19: Write Disable (WRDI) Sequence**

#### Enable-Write-Status-Register (EWSR)

The Enable-Write-Status-Register (EWSR) instruction arms the Write-Status-Register (WRSR) instruction and opens the status register for alteration. The Write-Status-Register instruction must be executed immediately after the execution of the Enable-Write-Status-Register instruction. This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like SDP (software data protection) command structure which prevents any accidental alteration of the status register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.



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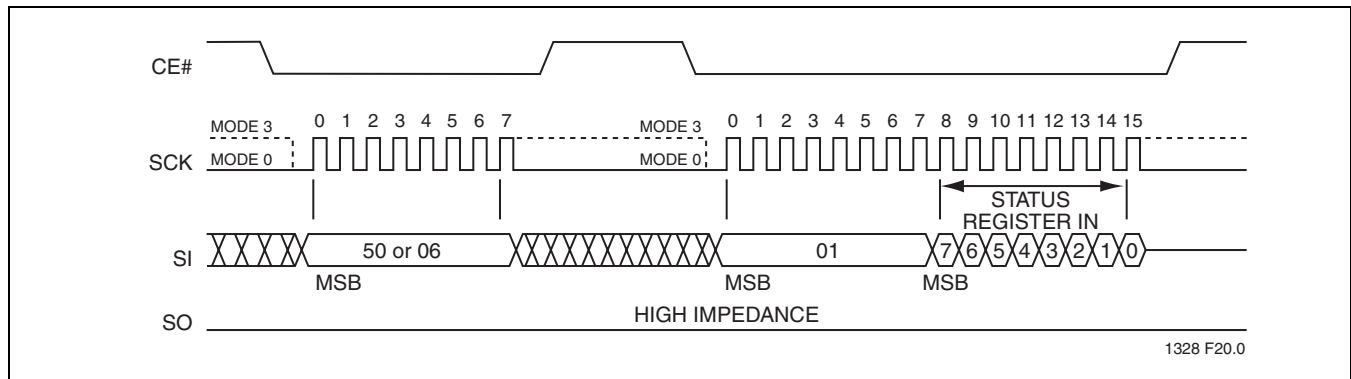
Advance Information

### Write-Status-Register (WRSR)

The Write-Status-Register instruction writes new values to the BP1, BP0, and BPL bits of the status register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 20 for EWSR or WREN and WRSR instruction sequences.

Executing the Write-Status-Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock-down the status register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL

bit is disabled and the SO, BPL, BP0, and BP1 bits in the status register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high ( $V_{IH}$ ) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the status register as well as altering the SO, BP0, and BP1 bits at the same time. See Table 3 for a summary description of WP# and BPL functions.

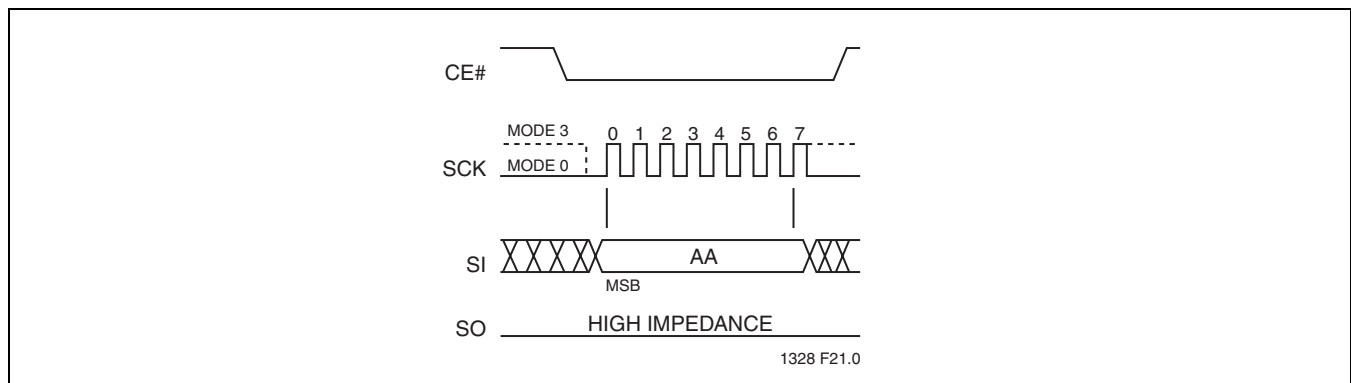


**FIGURE 20: Enable-Write-Status-Register (EWSR) or Write-Enable (WREN) and Write-Status-Register (WRSR) Sequence**

### Enable-Hold (EHL D)

The 8-bit command, AAH, Enable-Hold instruction enables the HOLD functionality of the RST#/HOLD# pin. CE# must remain active low for the duration of the Enable-Hold instruction sequence. The Enable-Hold instruction is initi-

ated by executing an 8-bit command, AAH. CE# must be driven high before the instruction is executed. See Figure 21 for the Enable-Hold instruction sequence.



**FIGURE 21: Enable-Hold Sequence**



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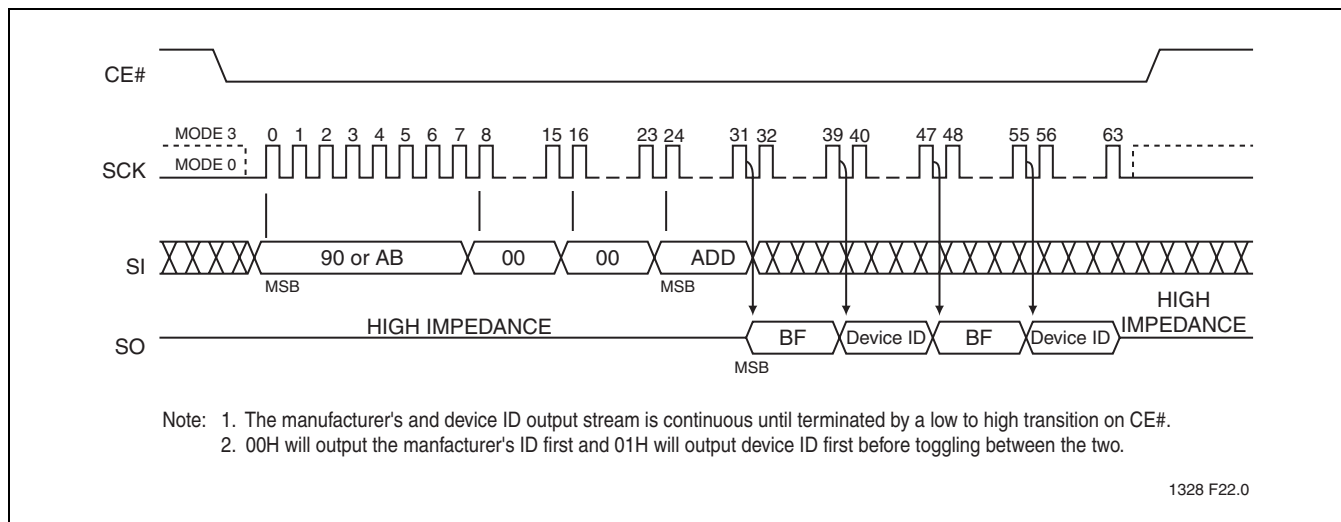
### Advance Information

### Read-ID

The Read-ID instruction identifies the manufacturer as SST and the device as SST25WF512/010/020. Use the Read-ID instruction to identify SST device when using multiple manufacturers in the same socket.

The device information is read by executing an 8-bit command, 90H or ABH, followed by address bits [A<sub>23</sub>-A<sub>0</sub>]. Following the Read-ID instruction, the manufacturer's ID is

located in address 000000H and the device ID is located in address 000001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on CE#.



**FIGURE 22: Read-ID Sequence**

**TABLE 10: Product Identification**

	Address	Data
Manufacturer's ID	000000H	BFH
Device ID		
SST25WF512	00001H	01H
SST25WF010	00001H	02H
SST25WF020	00001H	03H

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## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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### JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device as SST25WF512/010/020 and the manufacturer as SST. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. The Device ID is assigned by the manufacturer and con-

tains the type of memory in the first byte and the memory capacity of the device in the second byte. See Figure 23 for the instruction sequence. The JEDEC Read ID instruction is terminated by a low to high transition on CE# at any time during data output.

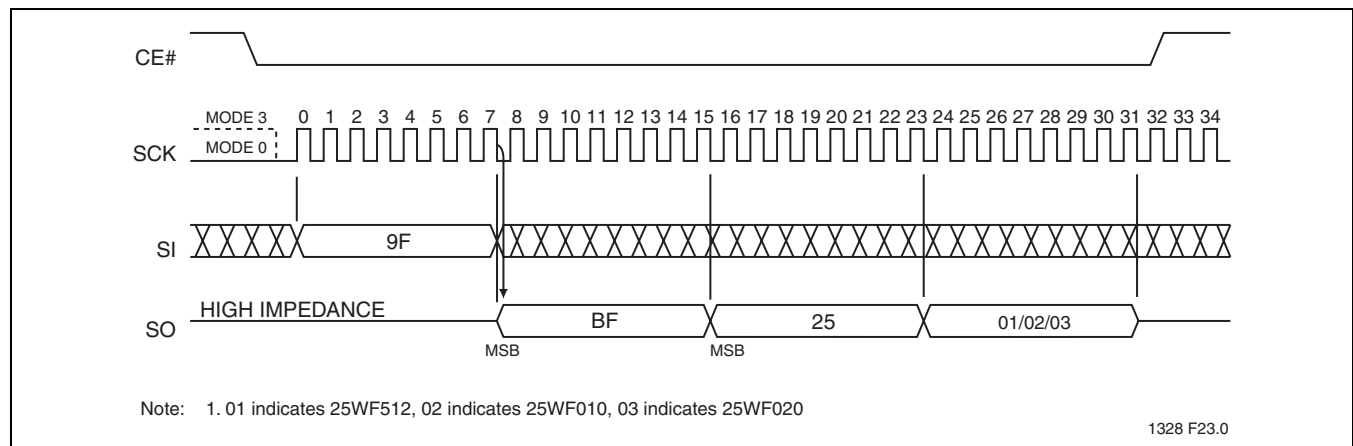


FIGURE 23: JEDEC Read-ID Sequence

TABLE 11: JEDEC Read-ID Data-Out for SST25WF512

Manufacturer's ID (Byte 1)	Device ID	
	Memory Type (Byte 2)	Memory Capacity (Byte 3)
BFH	25H	01H

T11.0 1328

TABLE 12: JEDEC Read-ID Data-Out for SST25WF010

Manufacturer's ID (Byte 1)	Device ID	
	Memory Type (Byte 2)	Memory Capacity (Byte 3)
BFH	25H	02H

T12.0 1328

TABLE 13: JEDEC Read-ID Data-Out for SST25WF020

Manufacturer's ID (Byte 1)	Device ID	
	Memory Type (Byte 2)	Memory Capacity (Byte 3)
BFH	25H	03H

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## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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### ELECTRICAL SPECIFICATIONS

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{DD}+0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to $V_{DD}+2.0V$
Package Power Dissipation Capability ( $T_A = 25^\circ C$ )	1.0W
Surface Mount Solder Reflow Temperature	260°C for 10 seconds
Output Short Circuit Current <sup>1</sup>	50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

#### OPERATING RANGE

Range	Ambient Temp	$V_{DD}$
Commercial	0°C to +70°C	1.65-1.95V
Industrial	-40°C to +85°C	1.65-1.95V

#### AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	$C_L = 30$ pF

### DC Characteristics

TABLE 14: DC Operating Characteristics

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
$I_{DDR}$	Read Current		15	mA	$CE\#=0.1 V_{DD}/0.9 V_{DD}@20$ MHz, SO=open
$I_{DDR2}$	Read Current		18	mA	$CE\#=0.1 V_{DD}/0.9V_{DD}@40$ Mhz, SO=open
$I_{DDW}$	Program and Erase Current		15	mA	$CE\#=V_{DD}$
$I_{SB}$	Standby Current		10	$\mu A$	$CE\#=V_{DD}$ , $V_{IN}=V_{DD}$ or $V_{SS}$
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT}=GND$ to $V_{DD}$ , $V_{DD}=V_{DD}$ Max
$V_{IL}$	Input Low Voltage		0.3	V	$V_{DD}=V_{DD}$ Min
$V_{IH}$	Input High Voltage	$0.7 V_{DD}$		V	$V_{DD}=V_{DD}$ Max
$V_{OL}$	Output Low Voltage		0.2	V	$I_{OL}=100$ $\mu A$ , $V_{DD}=V_{DD}$ Min
$V_{OH}$	Output High Voltage	$V_{DD}-0.2$		V	$I_{OH}=-100$ $\mu A$ , $V_{DD}=V_{DD}$ Min

T14.0 1328

TABLE 15: Capacitance ( $T_A = 25^\circ C$ ,  $f=1$  Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{OUT}^1$	Output Pin Capacitance	$V_{OUT} = 0V$	12 pF
$C_{IN}^1$	Input Capacitance	$V_{IN} = 0V$	6 pF

T15.0 1328

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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**TABLE 16: Reliability Characteristics**

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^1$	Endurance	10,000	Cycles	JEDEC Standard A117
$T_{DR}^1$	Data Retention	100	Years	JEDEC Standard A103
$I_{LTH}^1$	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T16.0 1328

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

## AC Characteristics

**TABLE 17: AC Operating Characteristics**

Symbol	Parameter	Limits - 20 MHz		Limits - 40 MHz		Units
		Min	Max	Min	Max	
$F_{CLK}^1$	Serial Clock Frequency		20		40	MHz
$T_{SCKH}$	Serial Clock High Time	20		11		ns
$T_{SCKL}$	Serial Clock Low Time	20		11		ns
$T_{SCKR}$	Serial Clock Rise Time		5		5	ns
$T_{SCKF}$	Serial Clock Fall Time		5		5	ns
$T_{CES}^2$	CE# Active Setup Time	20		8		ns
$T_{CEH}^2$	CE# Active Hold Time	20		8		ns
$T_{CHS}^2$	CE# Not Active Setup Time	10		10		ns
$T_{CHH}^2$	CE# Not Active Hold Time	10		10		ns
$T_{CPH}$	CE# High Time	100		100		ns
$T_{CHZ}$	CE# High to High-Z Output		20		19	ns
$T_{CLZ}$	SCK Low to Low-Z Output	0		0		ns
$T_{DS}$	Data In Setup Time	5		2		ns
$T_{DH}$	Data In Hold Time	5		5		ns
$T_{HLS}$	HOLD# Low Setup Time	10		8		ns
$T_{HHS}$	HOLD# High Setup Time	10		8		ns
$T_{HLH}$	HOLD# Low Hold Time	15		12		ns
$T_{HHH}$	HOLD# High Hold Time	10		10		ns
$T_{HZ}$	HOLD# Low to High-Z Output		20		20	ns
$T_{LZ}$	HOLD# High to Low-Z Output		20		20	ns
$T_{OH}$	Output Hold from SCK Change	0		0		ns
$T_V$	Output Valid from SCK		20		9	ns
$T_{SE}$	Sector-Erase		75		75	ms
$T_{BE}$	Block-Erase		75		75	ms
$T_{SCE}$	Chip-Erase		150		150	ms
$T_{BP}^3$	Byte-Program		60		60	$\mu$ s

T17.1 1328

1. Maximum clock frequency for Read instruction, 03H, is 20 MHz
2. Relative to SCK
3. AAI-Word Program TBP maximum specification is also at 60  $\mu$ s maximum time



# 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

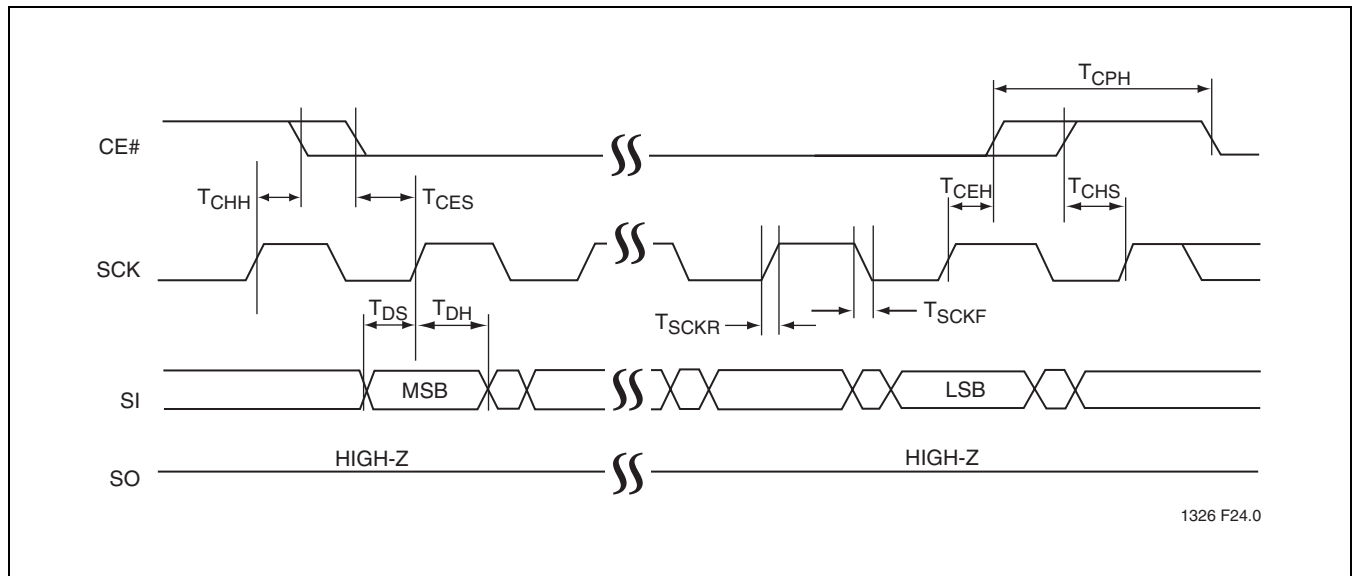
## Advance Information

**TABLE 18: Recommended System Power-up Timings**

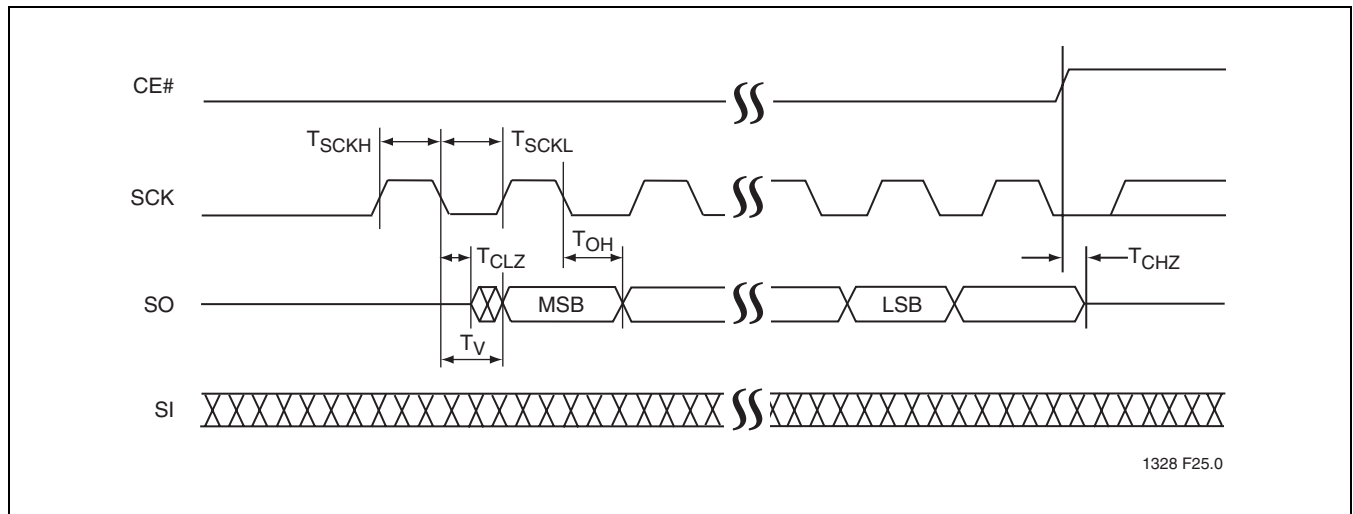
Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	$V_{DD}$ Min to Read Operation	100	$\mu s$
$T_{PU-WRITE}^1$	$V_{DD}$ Min to Write Operation	100	$\mu s$

T18.0 1328

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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**FIGURE 24: Serial Input Timing Diagram**


1328 F25.0

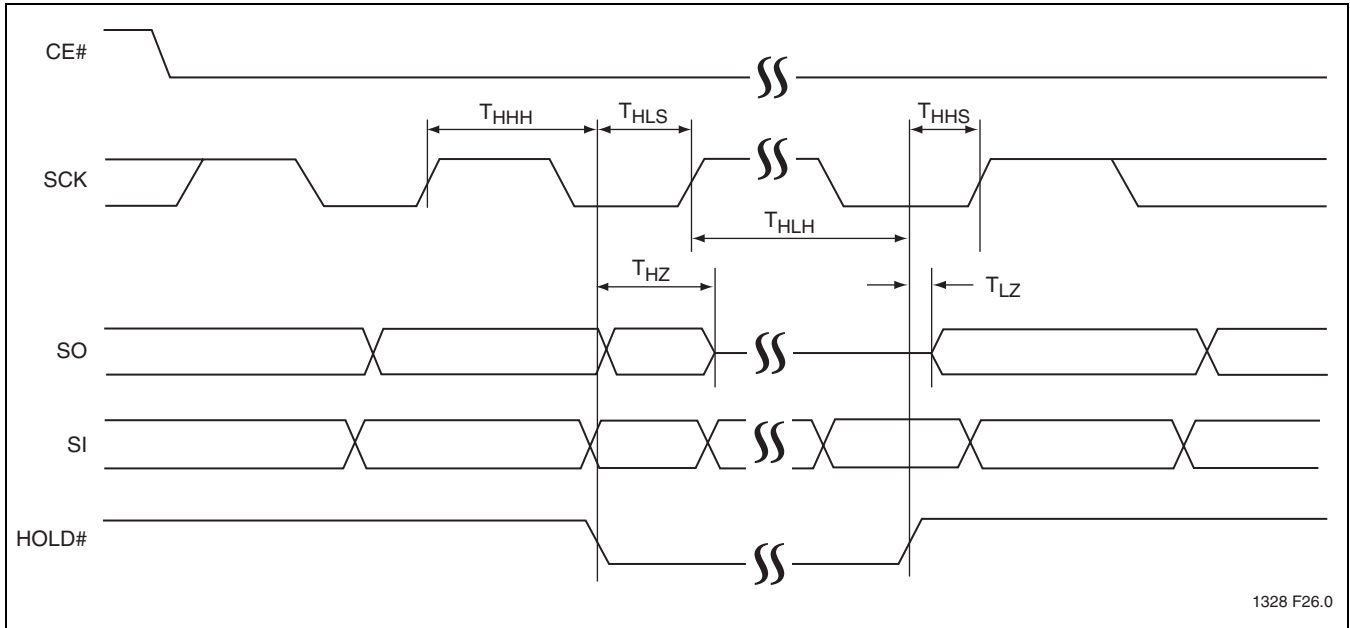
**FIGURE 25: Serial Output Timing Diagram**





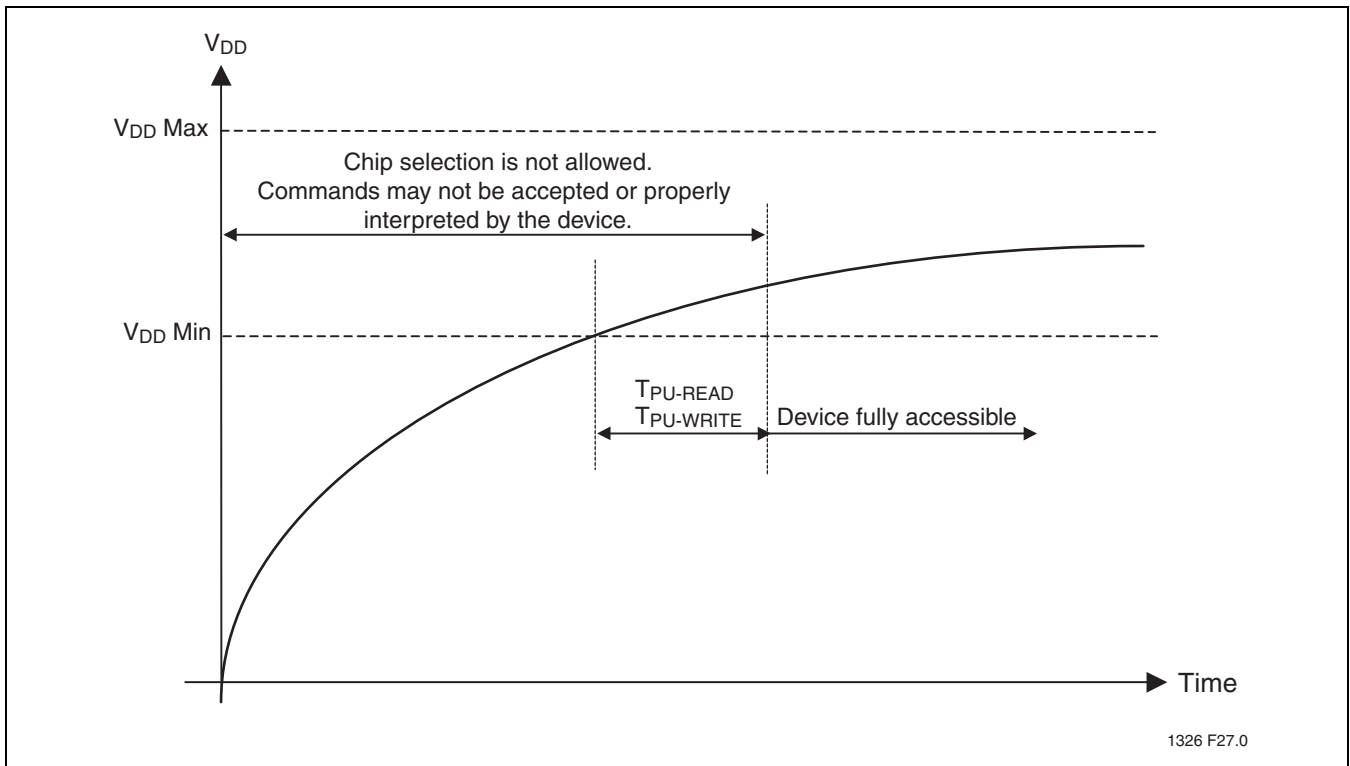
**512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash**  
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1328 F26.0

**FIGURE 26: Hold Timing Diagram**



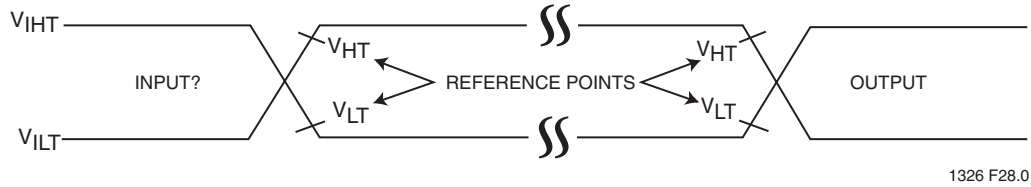
1326 F27.0

**FIGURE 27: Power-up Timing Diagram**



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

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AC test inputs are driven at  $V_{IHT}$  ( $0.9V_{DD}$ ) for a logic '1' and  $V_{ILT}$  ( $0.1V_{DD}$ ) for a logic '0'. Measurement reference points for inputs and outputs are  $V_{HT}$  ( $0.6V_{DD}$ ) and  $V_{LT}$  ( $0.4V_{DD}$ ). Input rise and fall times (10%  $\leftrightarrow$  90%) are <5 ns.

**Note:**  $V_{HT}$  -  $V_{HIGH}$  Test  
 $V_{LT}$  -  $V_{LOW}$  Test  
 $V_{IHT}$  -  $V_{INPUT HIGH}$  Test  
 $V_{ILT}$  -  $V_{INPUT LOW}$  Test

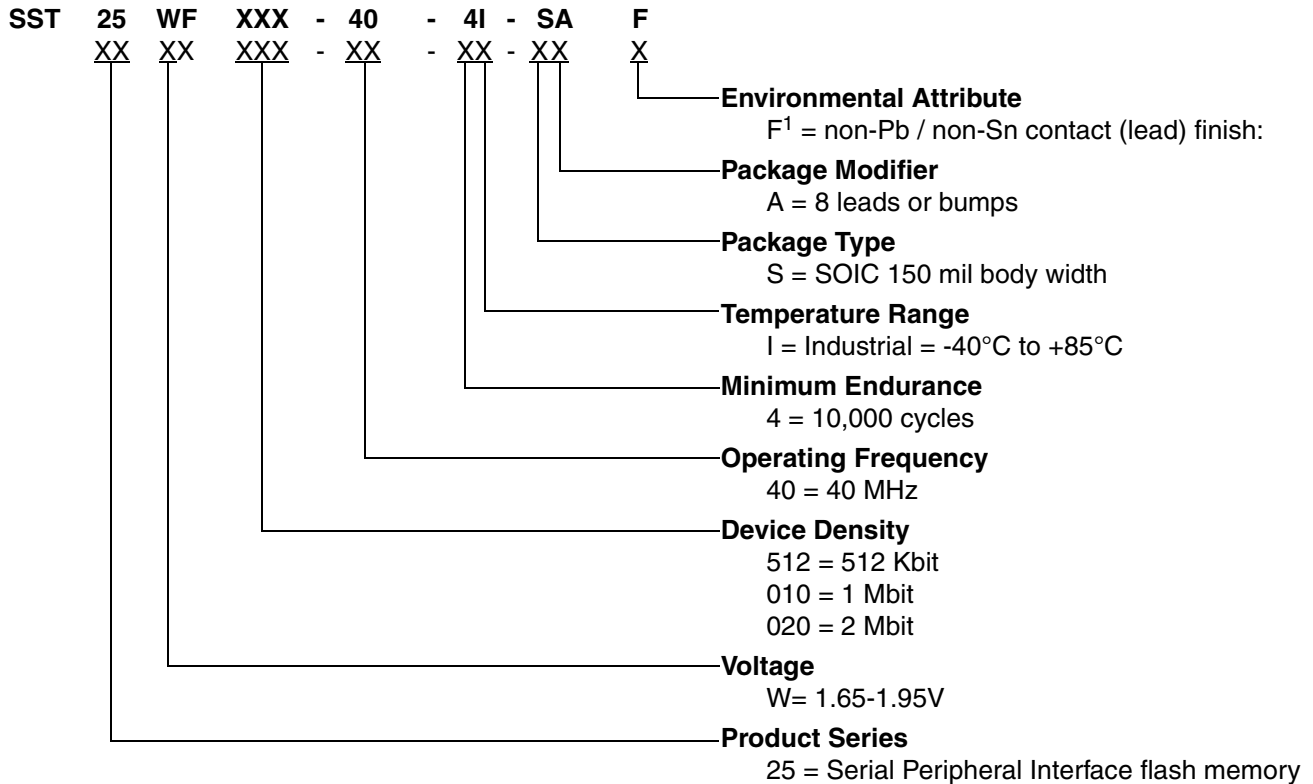
**FIGURE 28: AC Input/Output Reference Waveforms**



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

Advance Information

### PRODUCT ORDERING INFORMATION



1. Environmental suffix "F" denotes non-Pb/non-SN solder. SST non-Pb/non-Sn solder devices are "RoHS Compliant".

#### Valid combinations for SST25WF512

SST25WF512-40-4I-SAF

#### Valid combinations for SST25WF010

SST25WF010-40-4I-SAF

#### Valid combinations for SST25WF020

SST25WF020-40-4I-SAF

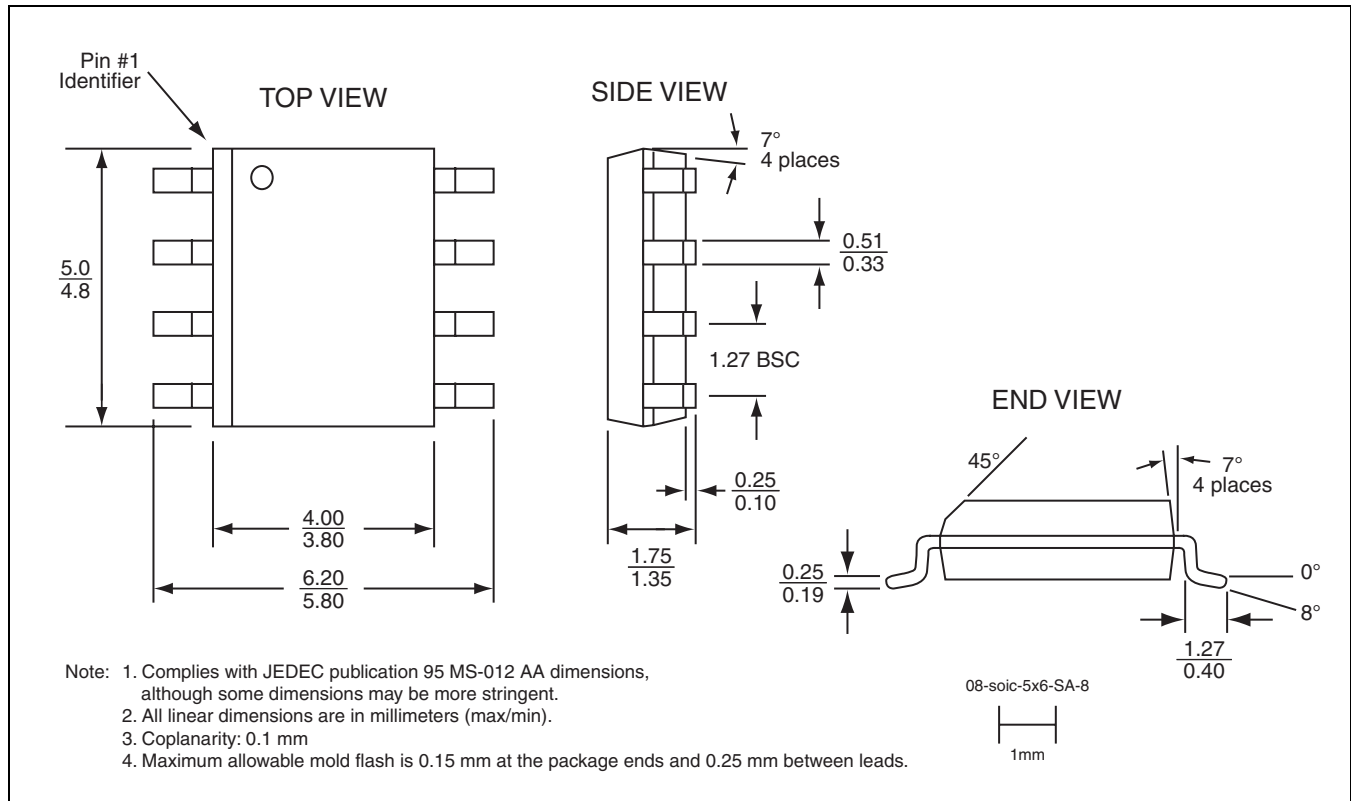
**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



## 512 Kbit / 1 Mbit / 2 Mbit 1.8V SPI Serial Flash SST25WF512 / SST25WF010 / SST25WF020

Advance Information

### PACKAGING DIAGRAMS



**FIGURE 29: 8-Lead Small Outline Integrated Circuit (SOIC)  
SST Package Code: SA**

**TABLE 19: Revision History**

Number	Description	Date
00	• Initial release of data sheet	Nov 2006